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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,859	07/15/2003	Lakhbeer S. Sidhu	A1064	9135

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G. VICTOR TREYZ
FLOOD BUILDING
870 MARKET STREET, SUITE 984
SAN FRANCISCO, CA 94102

EXAMINER	
MAI, ANH T	

ART UNIT	PAPER NUMBER
2832	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/620,859	SIDHU ET AL.
	Examiner	Art Unit
	Anh T. Mai	2832

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed January 3, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-33* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Sia et al. [6650220].

Sia discloses in figures 1-2 of prior art, a spiral stack inductor 22 having two metal-layer conductive lines 24/26, 24'/26' running parallel to each other in respective dielectric layer 20, 18; via-trench conductive line 22v between the two metal-layer conductive lines and eclectically connects the conductive lines [figure 1-2, column 4, lines 4-36].

> In the prior art, the spiral stacked inductor 22 is a two-turn stacked inductor. In FIG. 1 (PRIOR ART), are shown first and second turns 24 and 26.
> (6) A first connecting portion 30 having connecting vias 32 connects to the spiral stacked inductor 22 at one end and a second connecting portion 34 connects at the other end.
> (7) The first turn 24 has an inner diameter 36, a width 38 which is common to each of the turns, and a spacing 40 between each of the turns. The first connecting portion 30 passes under the two turns and thus is also referred to as an underpass 30.

(8) Referring now to FIG. 2 (PRIOR ART), therein is shown a cross-sectional view of the prior art on-chip inductor 10 along line 2--2 of FIG. 1 (PRIOR ART). The substrate 12 has the field dielectric layer 14 upon which a conductive material is deposited and patterned to form the underpass 30.
(9) The connecting ILD layer 16 is then deposited over the underpass 30. One or more first via openings are formed in the connecting ILD layer 16 connected to the underpass 30.
(10) A conductive material layer is deposited on the connecting ILD layer 16 and processed to form a first level of the spiral stacked inductor 22. When processed, first and second turns 24' and 26' of a first level 50' will be formed. The first via openings are also filled with conductive material to form connecting vias 32.
(11) The first level ILD layer 18 is then deposited over the first level 50'. One or more second via openings are formed in the first level ILD layer 18 connected to the first and second turns 24' and 26' along their lengths.
(12) A conductive material is deposited on the first level ILD layer 18 and processed to form the first and second turns 24 and 26 of a second level 50'. The first and second turns 24 and 26 are respectively connected to the first and second turn vias 24v and 26v along their lengths by the conductive material filling the respective vias openings to form first and second turn vias 24v and 26v.
(13) The second level ILD layer 20 is then deposited over the second level 50'.
(14) As will be understood by those skilled in the art, as a spiral stacked inductor has more turns, it will still have the same number of turns in each level and the turns will all be connected along their length by pluralities of vias.

With respect to claim 2, Sia discloses the copper as conductive material [figure 3].

In the described embodiment, the parallel spiral stacked inductor 122 is a parallel two-turn inductor. In FIG. 3, are shown first and second turns 124 and 126. Individually, the turns can be flat as shown or circular, and can be made from any conductive material including copper

With respect to claim 3, Sia discloses the spiral inductor has two ends connected to vias 32 and 133 [figure 3].

A first connecting portion 130 having connecting vias 132 connects to the parallel spiral stacked inductor 122 at one end and a second connecting portion 134 having connecting vias 133 connects at the other end.

With respect to claim 7, Sia discloses the via turns to correspond with inductor turn. It inherently means the conductor line and via line have the same length.

With respect to claims 8-9, "damascene and dual-damascene semiconductor fabrication process" has been considered but not given any patentable weight because it's a product by process claim. During the examination, the patentability of a product-by-process claim is determined by the novelty and nonobviousness of the claimed product itself without consideration of the process for making it which is recited in the claim. *In re Thorpe, 227 USPQ 964 (Fed cir. 1985).*

With respect to claim 10, the stack inductor having top dielectric layer 50' and top conductive line 24/26 is formed in the top dielectric layer [see figure 2].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Ewen [5446311].

Sia discloses the claimed invention as cited above except for three vertically aligned metal-layer conductive lines that run parallel to each other in the dielectric stack. Ewen discloses three vertically aligned conductive lines M1, M2, M3 run parallel to each other and at least two sets of via conductive lines 5, 9 electrically connecting three conductive lines [figure 3]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have additional levels of conductive layer as taught by Ewen to Sia. The motivation would have been to provide different configuration of the inductor as required by its function. Therefore, it would have been obvious to combine Ewen with Sia.

With respect to claim 11; the concave upper surface and convex lower surface are caused by dishing effect during the fabrication process as disclosed by applicant in the specs, page 4, lines 20-30.

5. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Tisharo et al. [5515022].

Sia discloses the claimed invention as cited above except for the via-trench having bottom width less than upper width. Tisharo discloses via 35 having cross shape shows the width of the upper is larger than that of the lower [figure 2; col 6, lines 30-39]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have tapering shape of the via as taught by Tisharo to Sia. The motivation would have been to improve large scale production and product yield and to reduce performance variation and change with time. Therefore, it would have been obvious to combine Tisharo with Sia.

> In the illustrated embodiment, the through-hole 4 has a diameter r.sub.0 on the first conductor pattern 31 bearing side which is larger than a diameter r.sub.1 on the rear side. Such tapering allows the through-hole 4 to be effectively filled with conductive paste simply by printing the paste while effecting suction from the rear side of the first magnetic material sheet 21. This leads to improved large-scale production, improved product yield, reduced performance variation, and reduced change with time.

6. Claims 13-14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Chi [6362012].

Sia discloses the claimed invention as cited above except for n-type/p-type wells at the surface of substrate that forms a plurality of reversed bias diodes that block eddy currents. Chi discloses the alternating regions of implanted n-well and p-well impurities in the substrate underneath the inductor or by reversing p-n junctions underneath the inductor to minimizing eddy currents [col 3, lns 11-16]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use n-well, p-well at the surface of semiconductor substrate as taught by Chi to Sia to reduce Eddy Current flowing in the substrate. Therefore, it would have been obvious to combine Chi with Sia.

With respect to claim 16, Sia in view of Chi does not disclose the size of the lateral spiral of less than 200 microns. It would have been obvious to select the dimension of the inductor as the matter of choice to satify the desired performance of the device. *In Gardner v. TEC Systems, Inc. , 725 F.2d 1338, 220 USPQ 777* (Fed.Cir. 1984),

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Chi et al. as applied in claim 13 above and further in view of Chen.

Sia in view of Chi disclose the claimed invention except for an region of trench isolation formed on the surface of the substrate. Chen discloses two metal-layer conductive lines 24, 28 in respective dielectric layers 25, 33; conductor 27 in via trench 26 in the dielectric stack that electrically connects the two conductive lines and region of shallow trench isolation 22 that formed on the surface of the substrate under the conductive lines [figures 2A-D; col 3, lines 5-45]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have region of isolation at the surface of semiconductor substrate as taught by Chen to Sia in view of Chi. The motivation would have been to increase spacing between the conductors and the substrate to reduce mutual inductance and skin effect [col 2, lines 65-68].

8. Claims 17-19, 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Gillespie et al. [6798039].

Sia discloses in figures 1-2 of prior art, a spiral stack inductor 22 having two metal-layer conductive lines 24/26, 24'/26' running parallel to each other in respective dielectric layer 20, 18; via-trench conductive line 22v between the two metal-layer conductive lines and eclectically connects the conductive lines [figure 1-2, column 4, lines 4-36].

Sia discloses the claimed invention as cited above except for n-type and p-type wells at the surface of semiconductor substrate beneath the spiral. Gillespie discloses in figures 4a-b, the n-type/p-type well regions positioned underneath the spiral inductor [col 7, lines 20-40] to reduce eddy current flowing in the substrate. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use n-well, p-well at the surface of semiconductor substrate as taught by Gillespie to Sia to reduce eddy current flowing in the substrate. Therefore, it would have been obvious to combine Gillespie with Sia.

> In FIG. 4A, a plan view of alternating N-type and P-type well regions 40 is provided. These alternating well regions provide a high resistance path in a semiconductor substrate (e.g., bulk semiconductor substrate). This high resistance path operates to reduce eddy currents within a semiconductor substrate when used in conjunction with an inductor according to an embodiment of the present invention. An exemplary inductor may include a plurality of primary strand segments 42 that are concentrically arranged. These N-type and P-type well regions are preferably elongate regions that extend in a lengthwise direction. This lengthwise direction is at least substantially orthogonal (e.g., .gtoreq.45.degree.) to the plurality of primary strand segments. In FIG. 4B, which represents an enlarged plan view of a portion of the alternating regions illustrated by FIG. 4A, the P-type well regions are illustrated as being electrically coupled together at multiple locations. These P-type well regions may be formed within a deeper N-type well region. Eddy current losses can also be reduced by defining an inductor using uppermost levels of metallization that are relatively distant from the substrate.

With respect to claims 22-25, the claims are method counterpart of product claims 17 - 20.

9. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Gellipie as applied to claim 17 above, and further in view of Ferraiolo et al. [5239289].

Sia in view of Gellipie disclose the claimed invention except for regular metal connect for conveying signals between devices on the IC. Ferraiolo discloses the metal connect 99 ends 151, 191 in circuit to other components [figures 1]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use a regular metal connect as taught by Ferraiolo to Sia in view of Gellippie to provide connection to other decives. Therefore, it would have been obvious to combine Gillespie with Sia.

FIG. 1 shows a substrate 100, which may be made of ceramic or of other suitable insulating material on which a conductor 99 is provided by any known method forming a spiral element 106 and ladder shaped elements 107, 108 and 109. The conductor 99 is attached at its ends 151 and 191, in-circuit to other components, usually disposed on or attached to the same substrate. The conductor 99 may be manufactured upon its own substrate and its ends attached to conductors upon another insulative support.

10. Claims 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Gillespie et al. as applied in claim 17 and further in view of Chi et al. [6362012].

Sia and Gillespie disclose the claimed invention claimed as cited above except for the material of via and conductive lines being copper. Chi uses copper as conductive material [col 9, lines 54-55] and copper damascene interconnects 27 [col 3, line 31]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to copper as conductive material as taught by Chi to Sia in view of Gillespie. The motivation would have been to minimize the resistivity of the conductive material. Therefore, it would have been obvious to combine Chi with Sia in view of Gillespie.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Gillespie et al. applied in claim 22 above, and further in view of Li et al. [2002/0177322A1]

Sia and Gillespie disclose the claimed invention except for "copper dual-damascene" fabrication process to form conductive lines. Li discloses the process of either single or dual-damascene process to fabricate multilevel structure containing vias and trenches [paragraph 12; figures 1A-D]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use dual-damascene process as taught by Li to Sia in view of Gillespie. The motivation would have been to facilitate manufacturing of the product having multilevel structures containing vias and trenches. Therefore, it would have been obvious to combine Li with Sia in view of Gillespie.

> Multi-level structures containing vias and trenches can be formed by successive application of either a single-damascene or a dual-damascene process, or a combination of both types of processes. For example, in any level having a trench, a via could also be formed (either before or after formation of the trench) resulting in a dual-damascene recess. This recess is then typically lined with a liner (which functions as a diffusion barrier for the conductive material) and then filled with a conductive material.

12. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Patel et al. [6429763].

Sia discloses in figures 1-2 of prior art, a spiral stack inductor 22 having two metal-layer conductive lines 24/26, 24'/26' running parallel to each other in respective dielectric layer 20, 18; via-trench conductive line 22v between the two metal-layer conductive lines and eclectically connects the conductive lines [figure 1-2, column 4, lines 4-36].

Sia discloses the claimed invention as cited above except for number spiral conductive lines is at least 3. Patel discloses multilayer plane magnetic device wherein spiral conductive lines are aligned in layers 1, 3, 5, 7 [see figure 9] parallel to each other. At the time of the invention, it would have to add another conductive spiral as taught by Patel to Sia to increase the inductance as required by certain functions of the device. Therefore, it would have been obvious to combine Patel with Sia.

13. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sia in view of Patel et al. as applied in claim 28 and further in view of Chi et al.

Sia and Gillespie disclose the claimed invention claimed as cited above except for the material of via and conductive lines being copper. Chi uses copper as conductive material [col 9, lines 54-55] and copper damascene interconnects 27 [col 3, line 31]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to copper as conductive material as taught by Chi to Sia in view of Patel. The motivation would have been

to minimize the resistivity of the conductive material. Therefore, it would have been obvious to combine Chi with Sia in view of Patel.

14. Claim 30 is rejected under 35 U.S.C. 35 U.S.C. 102(b) as being anticipated by Chen [6287931B1].

Chen discloses metal-layer conductive spiral line 28 in respective dielectric layers 29; conductor 27 in via trench 26 in the dielectric layer 25 of the stack that electrically connects the two conductive line with wire 24 [only one spiral shown in the drawings, but applicant discloses that two or more metal layers can be stacked to implement the spiral conductive layer 28]; region of shallow trench isolation 22 that formed on the surface of the substrate under the conductive lines [figures 2A-D; col 3, lines 5-45].

> A conductive layer is deposited, patterned and etched to be a wire 32 as shown in FIG. 2D. The wire 32 can be made of Al or Al--Cu alloy by means of PVD either directly filled into the via hole 30 in contact with the other end of the spiral conductive coil 28, or electrically connected to the other end of the spiral conductive coil 28 through a metal plug 31 of tungsten filled in the via hole 30.
>
> While the invention has been described with reference to various illustrative embodiments, the description is not intended to be construed in a limiting sense. For example, two or more metal layers can be stacked to implement the spiral conductive layers 28 to further lower series resistance Rs and thus increase the quality factor of the fabricated inductor. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as may fall within the scope of the invention defined by the following claims and their equivalents
>
> As shown in FIG. 2A, a photoresist layer 21 with predetermined patterns is formed on a semiconductor substrate 20 by means of photolithography to expose the portion on which a trench 22 to be formed. Usually, the semiconductor substrate 20 is a silicon substrate on which plural semiconductor devices, such as bipolar junction transistors and/or field-effect transistors, have been fabricated. For the purposes of simplicity, these have not been illustrated in the drawings. Then, the semiconductor substrate 20 is etched to shape the trench 22 by the patterned photoresist layer 22 as masking. Preferably, the etching procedure is performed by reactive ion etching (RIE) or high-density plasma etching (HDP) in the ambient of SF.sub.6 and O.sub.2. The trench 22 has a depth of about 2.about.100 .mu.m, and, preferably, 2.about.50 .mu.m.

15. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chi.

Chen discloses the claimed invention as cited above except for n-type/p-type wells at the surface of substrate that forms a plurality of reversed bias diodes that block eddy currents. Chi discloses the alternating regions of implanted n-well and p-well impurities in the substrate underneath the inductor or by reversing p-n junctions underneath the inductor to minimizing eddy currents [col 3, lns 11-16]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use n-well, p-well at the surface of semiconductor substrate as taught by Chi to Chen to reduce Eddy Current flowing in the substrate. Therefore, it would have been obvious to combine Chi with Chen.

16. Claims 32 -33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chi as applied in claim 31 above and further in view of Sia.

Chen in view of Chi discloses the claimed invention except for via line running parallel with the conductive lines. Sia discloses in figures 1-2 of prior art, a spiral stack inductor 22 having two metal-layer conductive lines 24/26, 24'/26' running parallel to each other in respective dielectric layer 20, 18; via-trench conductive line 22v between the two metal-layer conductive lines and eclectically connects the conductive lines [figure 1-2, column 4, lines 4-36]. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use via trench line as taught by Sia to Chen in view of Chi to provide connection along the length of the conductive lines. Therefore, it would have been obvious to combine Sia with Chen in view of Chi.

Allowable Subject Matter

17. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 recites inter alia, *a metal plate between the two metal layer conductive lines and the surface of the semiconductor substrate to reduce electromagnetic field interactions between the integrated circuit inductor and the semiconductor substrate.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh T. Mai whose telephone number is 571-272-1995. The examiner can normally be reached on 5/4/9 Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

am

ANH MAI
PRIMARY EXAMINER